

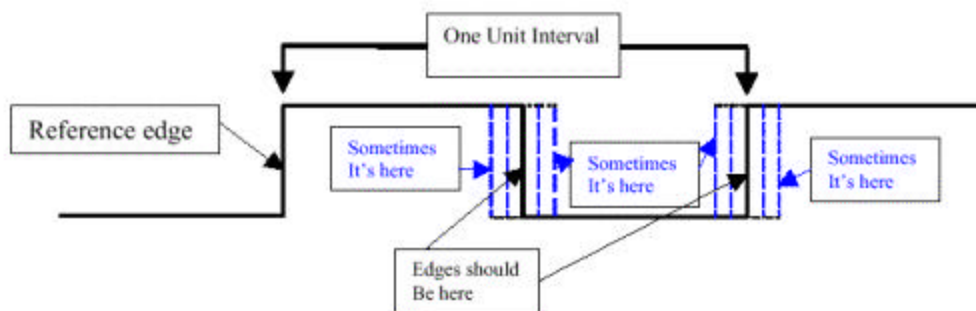


Jitter Test Results in Programmable Oscillators

This application note provides a clear understanding of jitter in programmable oscillators. It introduces definition, jitter measurements and actual data.

Jitter Definition

Jitter is short-term variations of the significant instants of a digital signal from their ideal positions in time.



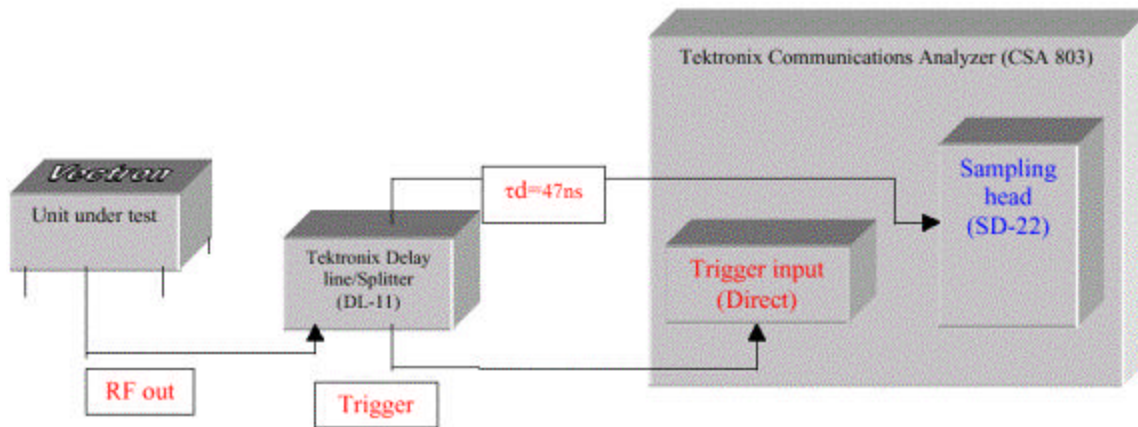
Digital Waveform with Jittered Edges

Jitter expressed in units of time describes the magnitude of the jitter in appropriate orders of magnitude, usually picoseconds. Period jitter and cycle to cycle jitter are the most widely used and understood in frequency control industry.

1. Period jitter is a standard measurement for the programmable oscillator. The period jitter consists of peak to peak period jitter and RMS (Root Mean Squared) period jitter. The peak to peak period jitter is the difference between the maximum and minimum of the clock signal. The RMS period jitter is the standard deviation of the peak to peak period jitter. We approximate peak to peak as 7σ , or 7 times the RMS value.
2. Cycle to cycle jitter is the difference between two adjacent cycles of the signal. The peak to peak period jitter is the worst case of cycle to cycle jitter.

Jitter Measurement

A true measure of clock jitter is the accurate position of clock edges over time. The most direct method of examining the placement of edges would be to look at the edges using an oscilloscope. Unfortunately, using standard oscilloscope techniques it is impossible to identify individual clock edges in absolute time. Any jitter measured with a standard oscilloscope is due to trigger instability. As a result, direct waveform measurements using oscilloscope (even a very good oscilloscope) are not a valid measurements of jitter. An additional technique is used to locate the reference edge, discriminate with time and examine the jitter on following edges. The picture below illustrates this method with a typical configuration.



Jitter Measurement

The output of the unit under test is fed into a splitter/delay line. The non-delayed output of the splitter is fed to the external trigger input of the oscilloscope (a CSA-803 in this case). The delayed output of the DL-11 is connected to the input of the oscilloscope. By examining the clock-stream at a time after trigger equal to the delay used (in this case 47 ns), the trigger-edge is located. After the trigger edge has been identified, the next edge is examined. A histogram plot is then produce of the measured jitter of the second edge. A CSA-803 is used for its statistical and histogram capabilities. This is a useful technique limited by the length of the delay line and the speed/sensitivity of the oscilloscope. This test method is appropriate when measuring oscillators that employ direct frequency multiplication or where low frequency jitter is not considered.

Jitter Test Results

Total jitter is a sum of unit jitter plus trigger jitter. VITE uses the total jitter as our specification.

$$(\text{Oscillator Jitter})^2 = (\text{Total Jitter})^2 - (\text{Trigger Jitter})^2$$

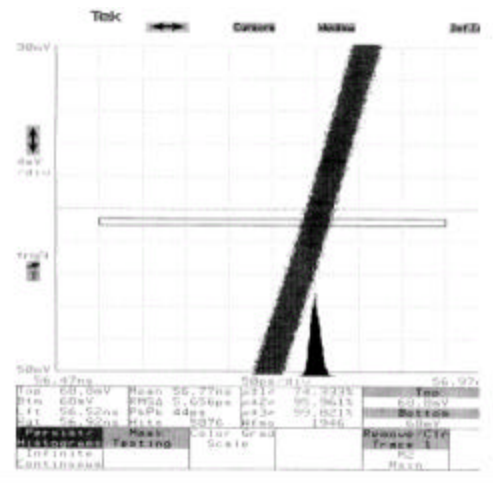
Oscillator Jitter = Jitter of the unit under test
 Total Jitter = Total measured jitter
 Trigger Jitter = Jitter of the test equipment

For example:

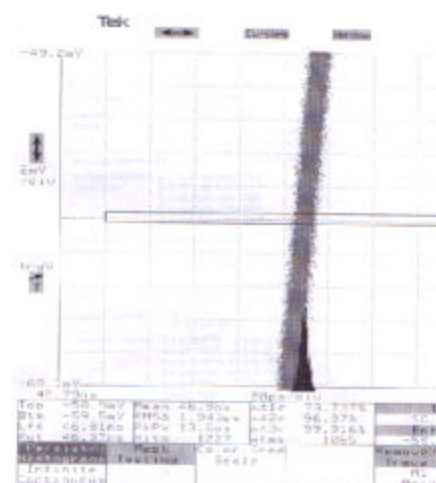
$$\text{Oscillator Jitter}^2 = 44.0^2 - 13.6^2$$

$$\text{Oscillator Jitter} = 41.8 \text{ ps peak to peak}$$

(VITE uses total jitter of 44.0 ps as peak to peak in data sheet).



Total Jitter = 44.0 ps peak to peak



Trigger Jitter = 13.6 ps peak to peak

An Example of Peak to Peak Period Jitter Measurement (VPB1-B3D-100M00)

The following table contains jitter information of the programmable oscillators in metal can, SMD ceramic and plastic package covered entire frequency range.

Frequency (MHz)	Jitter (ps peak to peak)		
	Metal Can 14 Pin Dip VPA1 3.3Vdc	C-type SMD Ceramic VPC1 3.3Vdc	Plastic SMD package VPE1 3.3Vdc
35.328	38	179	292
50.000	31	42	138
100.000	44	78	214
106.250	45	84	288
125.000	50	138	284
155.520	56	164	260

Actual Test Results in Peak to Peak Period Jitter

Frequency (MHz)	Jitter (ps RMS)		
	Metal Can 14 Pin Dip VPA1 3.3Vdc	C-type SMD Ceramic VPC1 3.3Vdc	Plastic SMD package VPE1 3.3Vdc
35.328	7	30	84
50.000	5	10	41
100.000	6	25	64
106.250	8	17	65
125.000	9	32	61
155.520	13	26	55

Actual Test Results in RMS Period Jitter

Jitter sometimes specified in \pm picoseconds (half of the actual data) because jitter deviation can be leading or lagging the center position.

Conclusion

The programmable oscillator can be programmed and re-programmed to every frequency immediately in contrast with the fixed oscillator built to specific frequency. The only difference is jitter which typically higher than fixed oscillator because programmable oscillator uses Phase Locked Loops (PLL) technologies to generate different frequencies. The clear understanding in the jitter performance can help our reader to select the right part at the right place.

Reference:

1. Joe Adler, Jitter in Clock Sources, Vectron International

Best regards,
Peter Sethakosee
VITE Quality